AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Cancelled)

2. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

a plurality of diffusion layer patterns formed on the semiconductor substrate;

an insulation film formed between the diffusion layer patterns on the semiconductor substrate; and

a through plug formed to have a side surface being in contact with the diffusion layer patterns, the side surface being ~~be partly~~ surrounded by the diffusion layer patterns without being in contact with the insulation film, and to pass through the diffusion layer patterns and the semiconductor substrate.

3. (Cancelled)

4. (Previously Presented) A semiconductor device as set forth in claim 7, further comprising a pattern portion formed above the diffusion layer patterns and/or the insulation film without being in contact with the through plug, the pattern portion using as a material thereof one kind selected from a group consisting of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), tantalum (Ta), and a chemical compound

composed of at least one metal out of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), and tantalum (Ta).

5. (Previously Presented) A semiconductor device as set forth in claim 2, further comprising a pattern portion formed above the diffusion layer patterns and/or the insulation film without being in contact with the through plug, the pattern portion using as a material thereof one kind selected from a group consisting of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), tantalum (Ta), and a chemical compound composed of at least one metal out of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), and tantalum (Ta).

6. (Previously Presented) A semiconductor device as set forth in claim 9,

wherein the at least one of the semiconductor chips further comprises a pattern portion formed above the diffusion layer patterns and/or the insulation film without being in contact with the through plug, the pattern portion using as a material thereof one kind selected from a group consisting of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), tantalum (Ta), and a chemical compound composed of at least one metal out of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), and tantalum (Ta).

7. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

a plurality of diffusion layer patterns formed on the semiconductor substrate;

an insulation film formed between the diffusion layer patterns on the semiconductor substrate to isolate the diffusion layer patterns from one another;

a pattern portion formed above the diffusion layer patterns and/or the insulation film, the pattern portion using as a material thereof one kind selected from a group consisting of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), tantalum (Ta), and a chemical compound composed of at least one metal out of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), and tantalum (Ta); and

a through plug formed to have a side surface being in contact with the insulation film, the side surface being ~~be partly~~ surrounded by the insulation film without being in contact with the diffusion layer patterns, and to pass through the insulation film and the semiconductor substrate, the through plug being partly surrounded [[also]] by the pattern portion above the diffusion layer patterns and/or the insulation film and being insulated from the pattern portion.

8. (Previously Presented) A semiconductor device as set forth in claim 2, further comprising a pattern portion formed above the diffusion layer patterns and/or the insulation film, the pattern portion using as a material thereof one kind selected from a group consisting of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), tantalum (Ta), and a chemical compound composed of at least one metal out of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), and tantalum (Ta),

wherein the through plug is partly surrounded also by the pattern portion above the plurality of diffusion layer patterns and/or the insulation film.

9. (Currently Amended) A semiconductor device comprising:

a plurality of semiconductor chips, at least one of the semiconductor chips including:

a semiconductor substrate;

a plurality of diffusion layer patterns formed on the semiconductor substrate;

an insulation film formed between the diffusion layer patterns on the semiconductor substrate to isolate the diffusion layer patterns from one another;

a pattern portion formed above the diffusion layer patterns and/or the insulation film, the pattern portion using as a material thereof one kind selected from a group consisting of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), tantalum (Ta), and a chemical compound composed of at least one metal out of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), and tantalum (Ta); and

a through plug formed to have a side surface being in contact with the insulation film, the side surface being ~~be partly~~ surrounded by the insulation film without being in contact with the diffusion layer patterns, and to pass through the insulation film and the semiconductor substrate, the through plug being partly surrounded [[also]] by the pattern portion above the diffusion layer patterns and/or the insulation film and being insulated from the pattern portion, or a through plug formed to have a side surface being in contact with the insulation film, the side surface being ~~be partly~~ surrounded by the diffusion layer patterns

without being in contact with the insulation film, and to pass through the diffusion layer patterns and the semiconductor substrate; and

a connecting member electrically connecting the through plugs of the at least one of the semiconductor chips to at least one of the semiconductor chips.

10. (Previously Presented) A semiconductor device as set forth in claim 7, wherein each of the diffusion layer patterns has a metal silicide layer.

11. (Previously Presented) A semiconductor device as set forth in claim 2, wherein each of the diffusion layer patterns has a metal silicide layer.

12. (Previously Presented) A semiconductor device as set forth in claim 9, wherein each of the diffusion layer patterns has a metal silicide layer.

13. (Previously presented) A semiconductor device as set forth in claim 7, wherein the through plug has a columnar electric conductor made of copper and an insulation layer made of any one of silicon oxide, silicon nitride, and a combination of silicon oxide and silicon nitride, the insulation layer surrounding the columnar electric conductor.

14. (Original) A semiconductor device as set forth in claim 2, wherein the through plug has a columnar electric conductor made of copper and an insulation layer

made of any one of silicon oxide, silicon nitride, and a combination of silicon oxide and silicon nitride, the insulation layer surrounding the columnar electric conductor.

15. (Previously presented) A semiconductor device as set forth in claim 9, wherein the through plug has a columnar electric conductor made of copper and an insulation layer made of any one of silicon oxide, silicon nitride, and a combination of silicon oxide and silicon nitride, the insulation layer surrounding the columnar electric conductor.

16. (Previously Presented) A semiconductor device as set forth in claim 7, wherein a diameter of the through plug is larger than an interval between adjacent ones of the diffusion layer patterns.

17. (Previously Presented) A semiconductor device as set forth in claim 2, wherein a diameter of the through plug is larger than an interval between adjacent ones of the diffusion layer patterns.

18. (Previously Presented) A semiconductor device as set forth in claim 9, wherein a diameter of the through plug is larger than an interval between adjacent ones of the diffusion layer patterns.

19. (Previously Presented) A semiconductor device as set forth in claim 7, wherein a diameter of the through plug is larger than a size of at least one of the diffusion layer patterns.

20. (Currently Amended) A semiconductor device as set forth in claim 9,

wherein the through plug is formed to have a side surface being in contact with the insulation film, the side surface being ~~be partly~~ surrounded by the insulation film without being in contact with the diffusion layer patterns, and to pass through the insulation film and the semiconductor substrate, the through plug being partly surrounded [[also]] by the pattern portion above the diffusion layer patterns and/or the insulation film and being insulated from the pattern portion, and

wherein a diameter of the through plug is larger than a size of at least one of the diffusion layer patterns.

21. (Previously Presented) A semiconductor device as set forth in claim 2,

wherein the insulation film is formed to isolate the diffusion layer patterns from one another.

22. (Previously Presented) A semiconductor device as set forth in claim 2, wherein the diffusion layer patterns are dummy diffusion layer patterns.

23. (Previously Presented) A semiconductor device as set forth in claim 7, wherein the diffusion layer patterns are dummy diffusion layer patterns.

24. (Previously Presented) A semiconductor device as set forth in claim 9, wherein at least one of the diffusion layer patterns of the at least one of the semiconductor chips is a dummy diffusion layer pattern.